Question Paper Code : X 10356

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020/
APRIL/MAY 2021

Third/Fourth Semester

Electronics and Communication Engineering

EC 8392 – DIGITAL ELECTRONICS

(Common to Biomedical Engineering/B.E. Computer and Communication Engineering/
Mechatronics Engineering/Medical Electronics/B.E. Robotics and Automation)

(Regulations 2017)

Time : Three Hours   Maximum : 100 Marks

Answer ALL questions

PART – A   (10×2=20 Marks)

1. Convert $[643]_{10}$ into its Excess 3-code.

2. Express the function Y = A + BC in canonical POS.

3. Write notes on full adder.

4. Define binary decoder.

5. Show how S-R flip flop is converted into D-flip flop.

6. What is shift register ?

7. Draw a block diagram of asynchronous sequential circuits.

8. Outline hazard and static 1 hazard.

9. Interpret about programmable logic array and infer how it differs from ROM.

10. What do you mean by propagation delay and noise margin ?

PART – B   (5×13=65 Marks)

11. a) i) Find the MSOP representation for F(A, B, C, D, E) = m(1, 5, 7, 13, 14, 15, 17, 18, 21, 22, 25, 29) + d(6, 9, 19, 23, 30) using K-Map method. Draw the circuit of the minimal expression using only NAND gates.   **(8)**

    ii) Show that if all the gate in a two – level OR-AND gate network are replaced by NOR gate, the output function does not change.   **(5)**

(OR)

    b) What are the advantages of using tabulation method ? Determine the Minimal Sum Of Products for the Boolean expression F = $\sum$(1, 2, 3, 7, 8, 9, 10, 11, 14, 15) using Tabulation method.   **(13)**

12. a) i) Design and explain the 1 to 8 Demultiplexer. **(8)**

  ii) Interpret Octal to Binary Encoder in brief. **(5)**

(OR)

  b) Illustrate how two 4-bit numbers are compared using magnitude comparator. **(13)**

13. a) i) Summarize the operation of JK flip-flop with neat diagram. **(7)**

  ii) Explain the operation of Master slave flip flop and show how the race around condition is eliminated. **(6)**

(OR)

  b) Explain the operation of synchronous three bit counter. **(13)**

14. a) Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. When $X_1 = 0$, the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0. **(13)**

(OR)

  b) Critically examine cycles and races in asynchronous sequential circuits. **(13)**

15. a) Draw the basic circuit of a ROM cell and describe its working principle with its architecture. **(13)**

(OR)

  b) Present the basic concepts of PLA and its applications. **(13)**

PART – C   **(1×15=15 Marks)**

16. a) Analyze the working principle and characteristics of CMOS (i) Inverter (ii) NAND gate (iii) NOR gate with circuit diagram. **(15)**

(OR)

  b) Explain the working principle of (i) TTL NAND gate (ii) ECL OR/NOR gate with circuit diagram. **(15)**

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